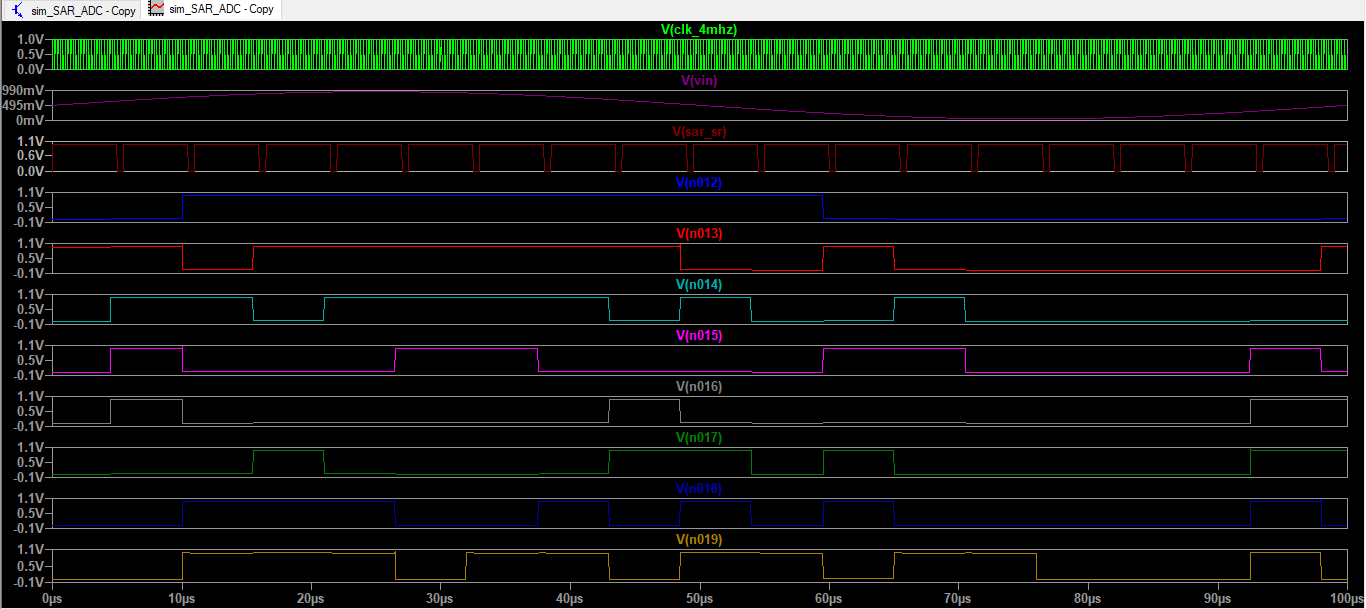
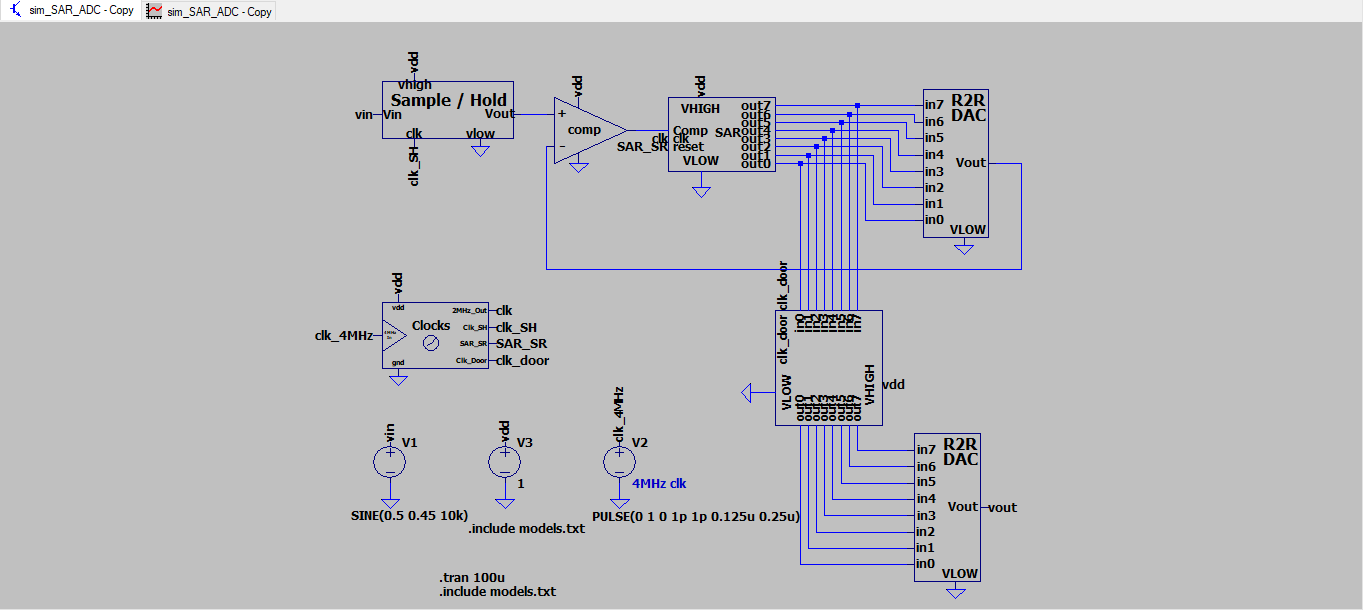
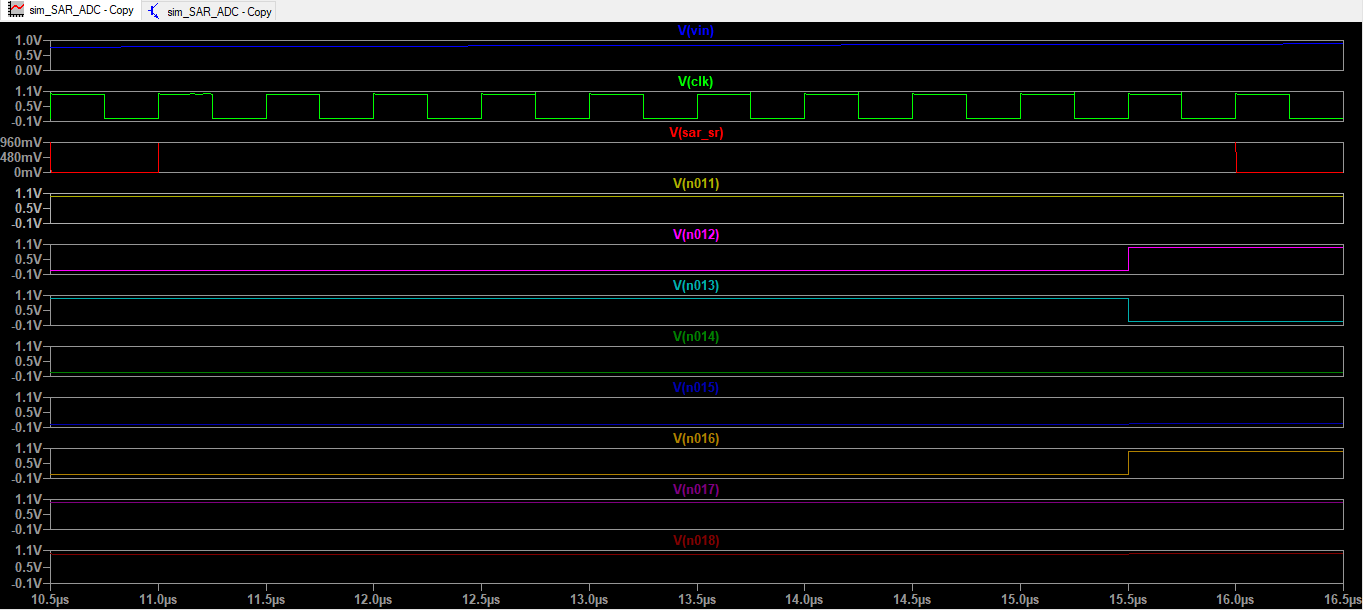
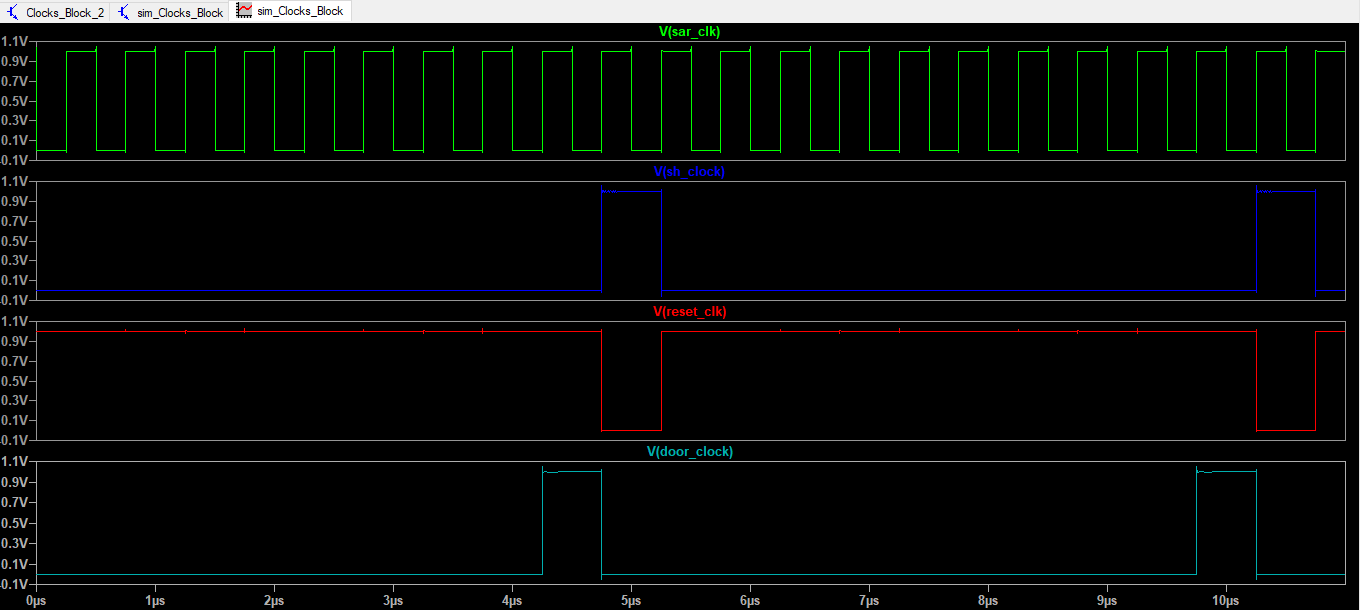
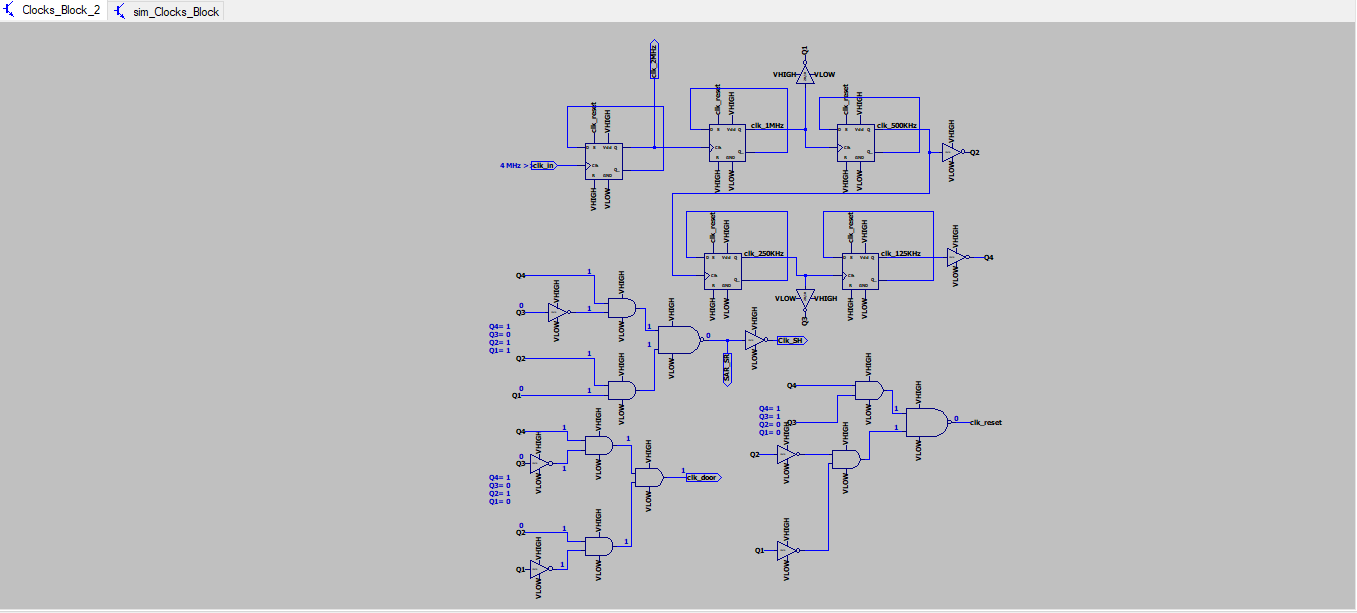
**SAR ADC**



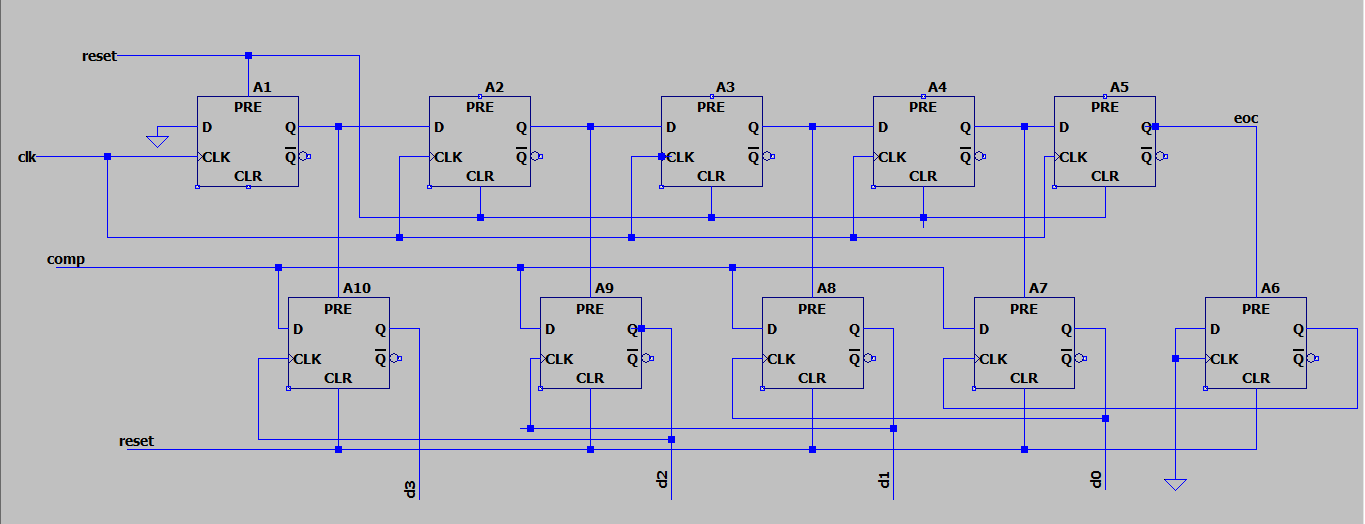
**SAR ADC PLOTS**

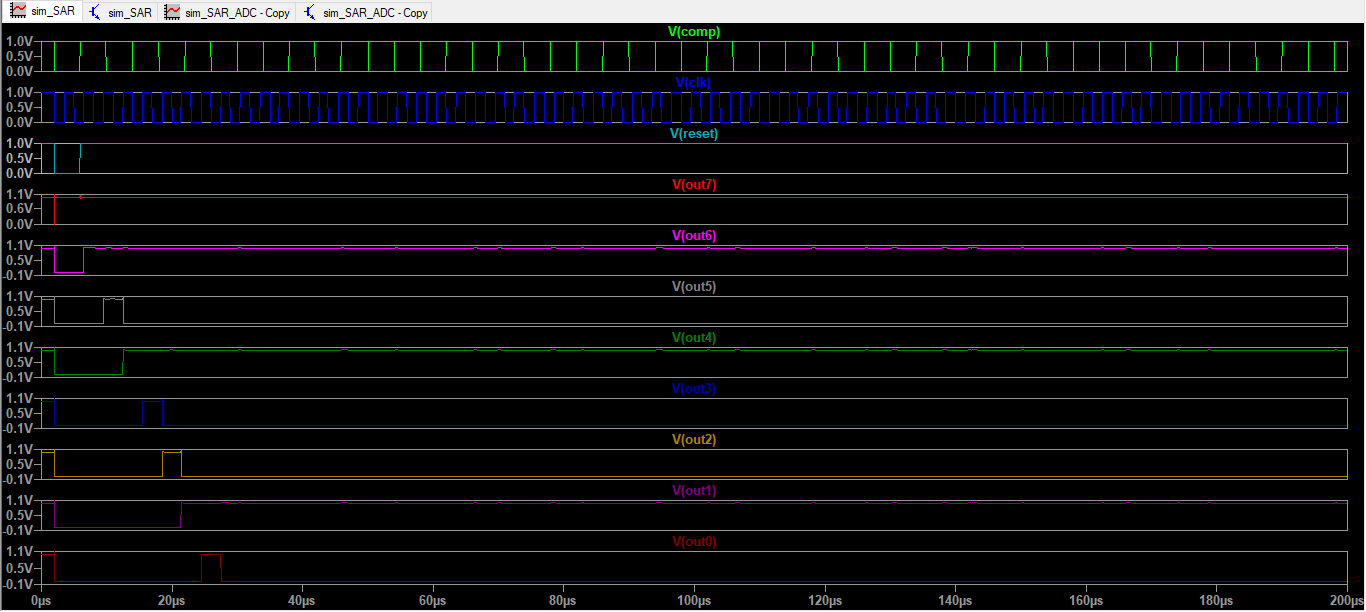


**Clock Generator**

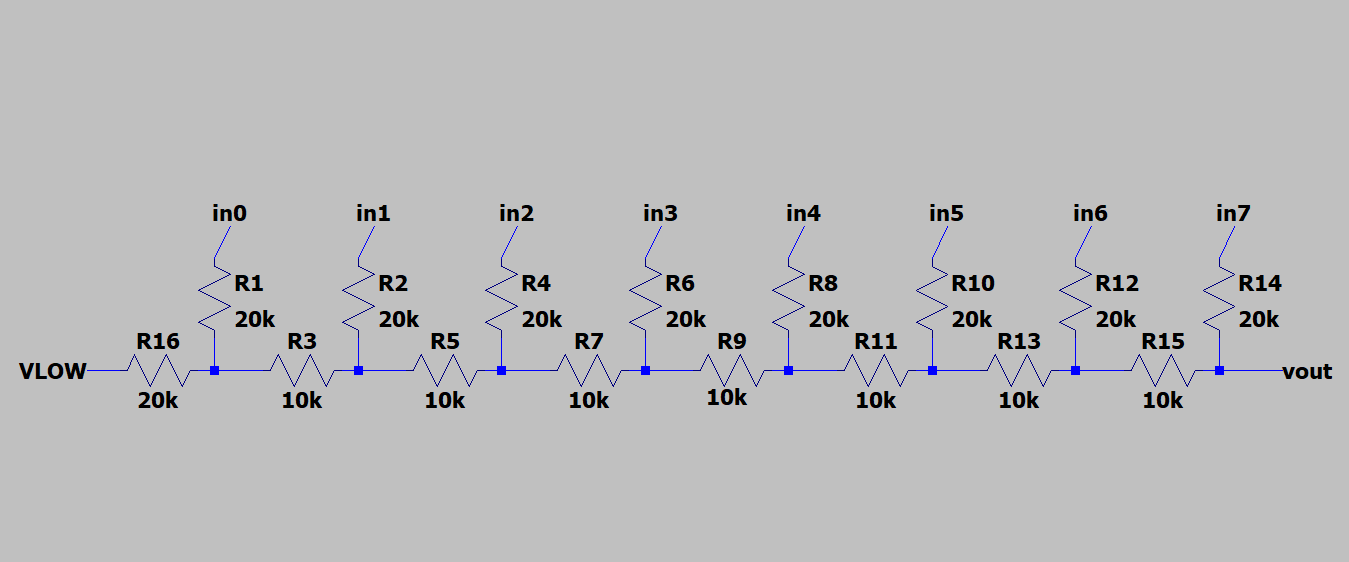
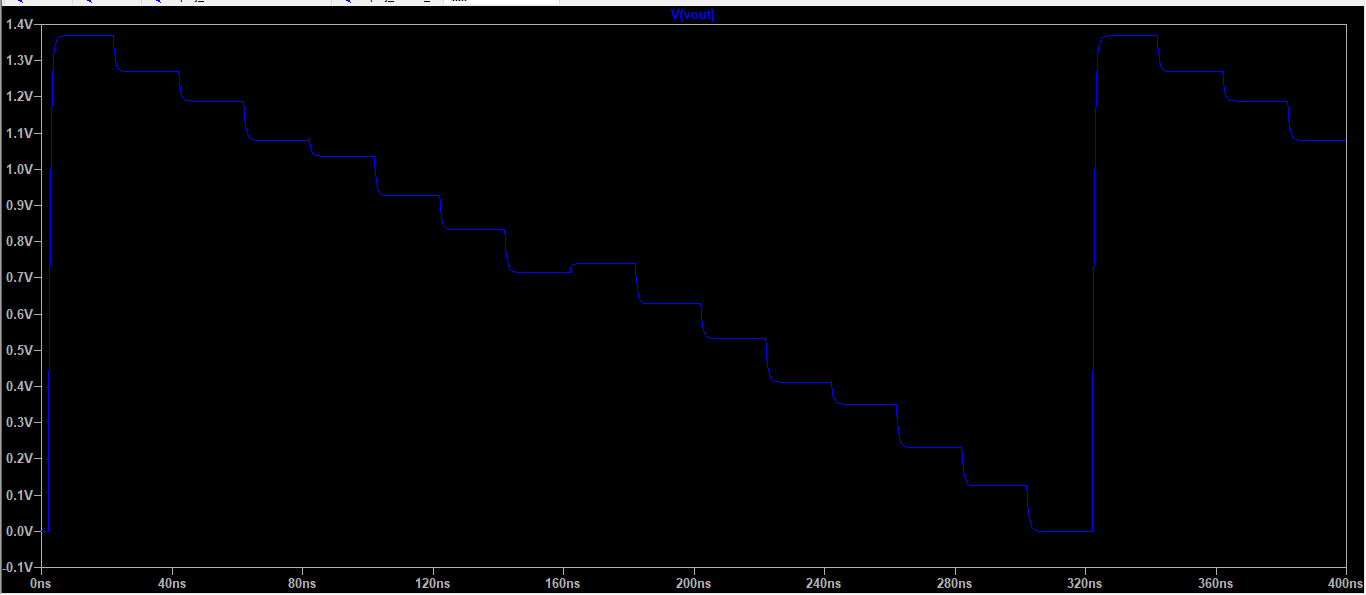


**SAR logic Block**

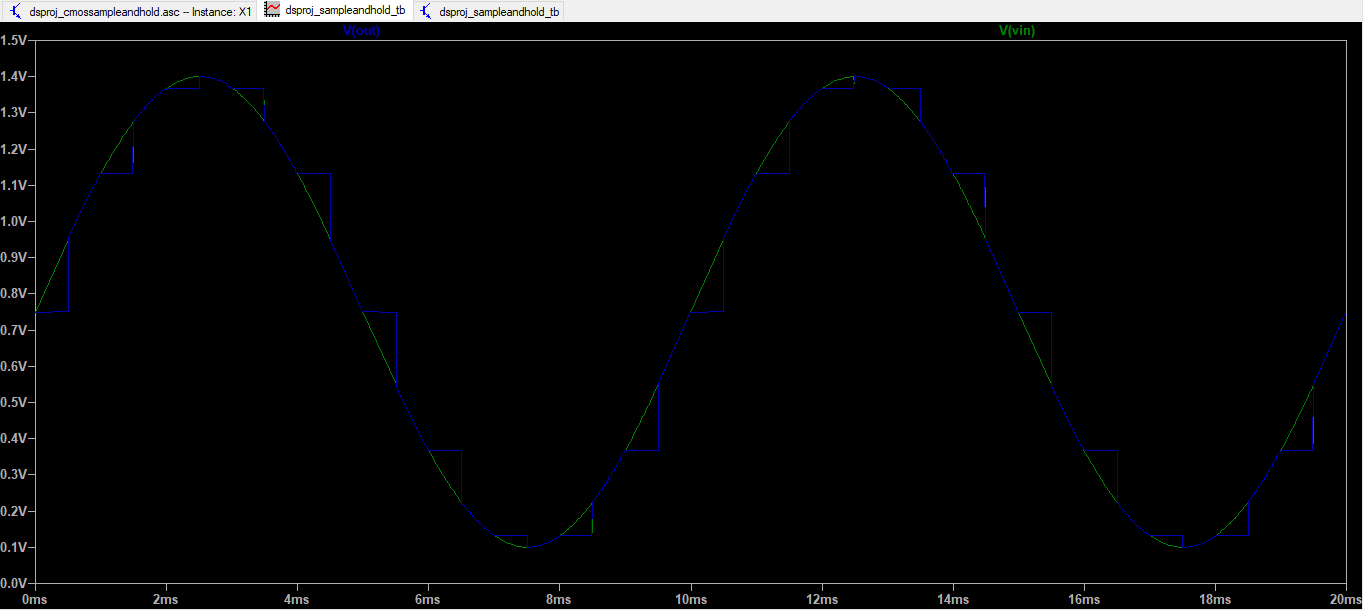
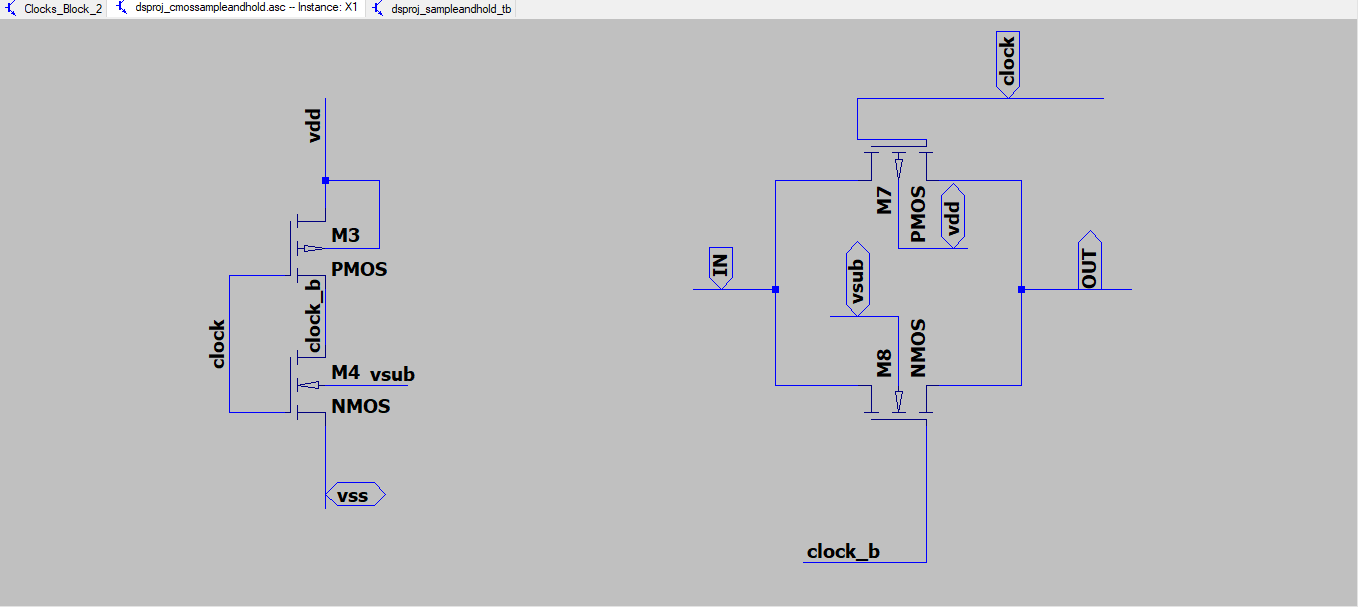


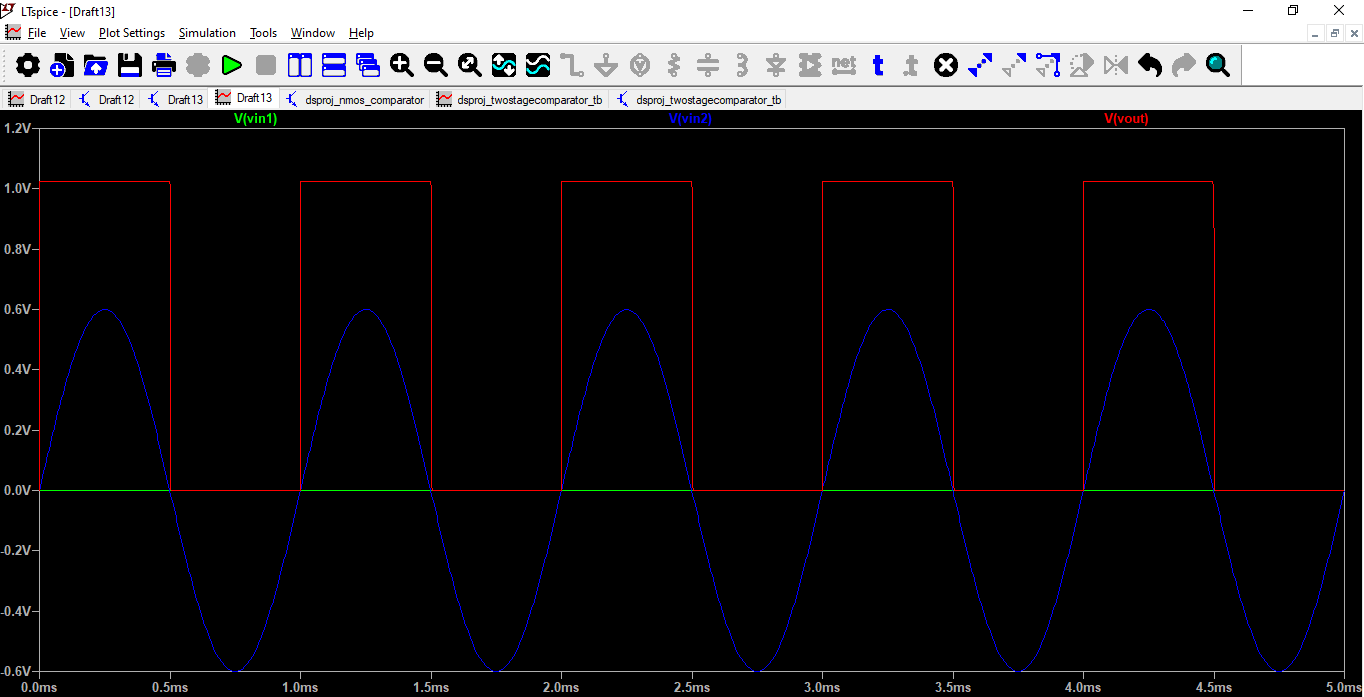
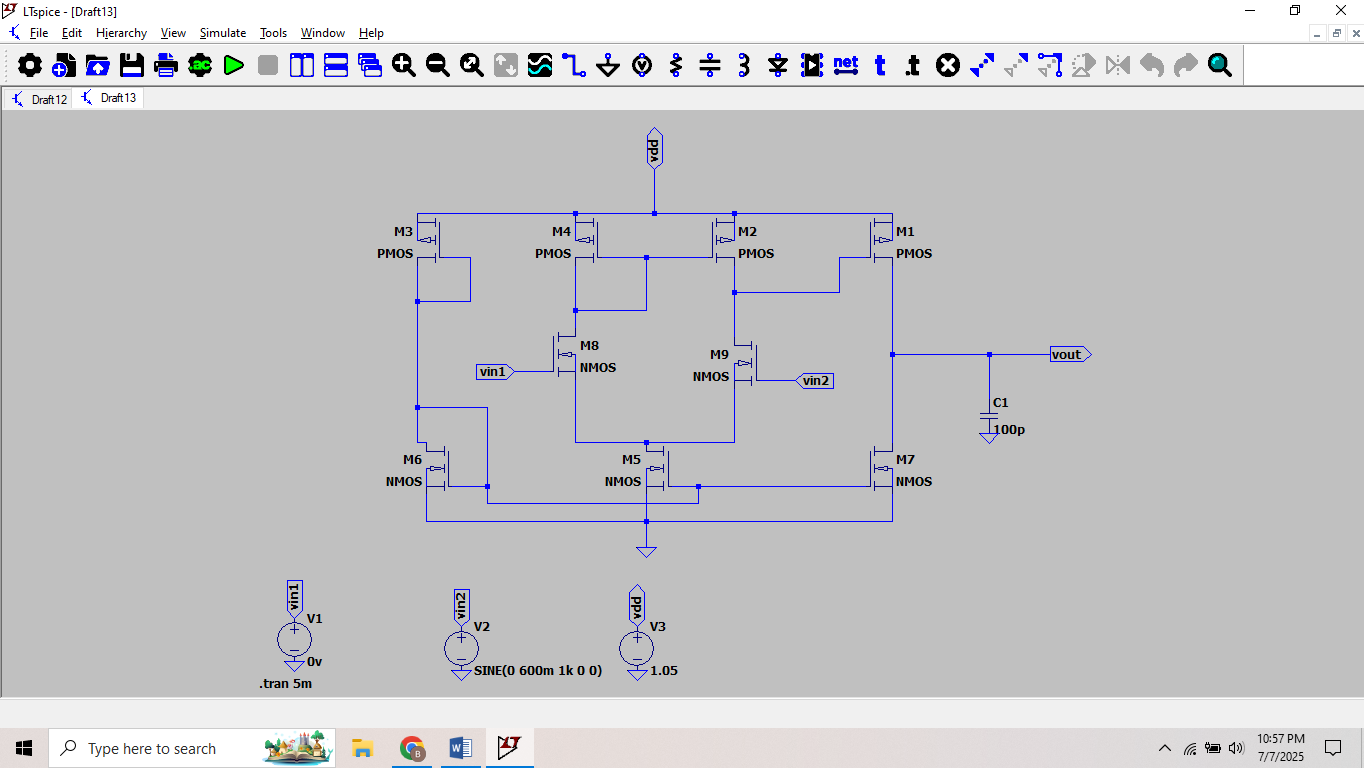


**R2R Ladder type DAC**



**Sample and Hold Circuit**



**Two stage comparator**